CLAIMS:

1. A processor (10) having a processing pipeline (100), the processor (10) comprising:

loop end detection means (114a, 144) for detecting a loop end to generate detection information; and

a control stage (142) for controlling a loop execution dependent on the detection information;

characterized by further comprising:

a loop start detection unit (116a) for detecting a loop start instruction, the loop end detection means (114a, 144) being responsive to the loop start detection unit (116a), and the loop start detection unit (116a) preceding the control stage (142) in the processing pipeline (100).

2. A processor (10) as claimed in claim 1, characterized in that the loop end detection means (114a, 144) comprise:

a loop end detection unit (114a) preceding the loop start detection unit (116a) in the processing pipeline (100) for detecting a loop end to generate a detection tag; and

a tag detection unit (144) for detecting the detection tag to provide the detection information to the control stage (142).

3. A processor (10) as claimed in claim 2, characterized in that the detection tag comprises a first bit indicating a first loop end, and a second bit indicating a second loop end.

4. A processor (10) as claimed in claim 2, characterized by further comprising storage means (200) for storing the detection tag.

5. A processor (10) as claimed in claim 4, characterized in that the storage means (200) comprise an additional pipeline (200) at least comprising a first additional pipeline stage (216) corresponding with a first intermediate stage (116) of the processing pipeline and

a second additional pipeline stage (222) corresponding with a second intermediate stage (122) of the processing pipeline (100).

6. A processor (10) as claimed in claim 1, characterized in that the processing pipeline (100) comprises a fetch stage (112) responsive to the loop end detection means (114a), said fetch stage (112) comprising:

further storage means (194) for storing loop instruction information; and

a program counter (192) coupled to the further storage means (194).

7. A processor as claimed in claim 1, characterized by further comprising control circuitry (146) responsive to the control stage (142) for manipulating a stage (112; 114; 116; 122; 124) of the processing pipeline (100).

8. A processor (10) as claimed in claim 7 characterized in that the control circuitry (146) comprises an interrupt handler (30).

9. A processor (10) as claimed in claim 1, characterized by comprising further control circuitry (132) responsive to the loop start detection means (116a) for forcing an instruction into the processing pipeline (100).

10. A processor (10) as claimed in claim 1, characterized by comprising a further pipeline (300) at least comprising a first further stage (312) corresponding with a first stage (112) of the processing pipeline (100), and a second further stage (314) corresponding with a second stage (114) of the processing pipeline (100).

11. A method of executing instruction loops in a processor (10) having a processing pipeline (100), the method comprising the following steps:

detecting a loop end to generate detection information;

controlling a loop execution dependent on the detection information;

characterized by:

detecting a loop start instruction, the step of detecting a loop end being responsive to the step of detecting a loop start instruction, both steps of detecting a loop end and detecting a loop start instruction taking place before controlling a loop execution.